R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found in the specification, for example, on page 4 lines 24-28 and FIG. 3, as originally filed. Thus, no new matter has been added.

OBJECTION TO THE DRAWINGS

The objection to the drawings is respectfully traversed and should be withdrawn. Claim 21 does not provide an encoder receiving a video signal from a frame buffer as alleged on page 6 of the Office Action. Regarding claim 28, FIG. 6 of the application illustrates an encoder 82 receiving video from a frame buffer 80. As such, the objection to the drawings should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-5, 7-10, 24 and 25 under 35 U.S.C. §103(a) as being unpatentable over O'Connor '667 in view of Yonemitsu et al '840 (hereafter Yonemitsu) has been obviated in part, is respectfully traversed in part, and should be withdrawn.

The rejection of claim 11 under 35 U.S.C. §103(a) as being unpatentable over O'Connor and Yonemitsu in further view of Russo '383 is respectfully traversed and should be withdrawn.

The rejection of claims 14, 20, 22 and 27 under 35 U.S.C. §103(a) as being unpatentable over O'Connor is respectfully traversed and should be withdrawn.

The rejection of claims 15, 16, 18, 19, 21, 23, 28 and 29 under 35 U.S.C. §103(a) as being unpatentable over Thomason et al. '612 (hereafter Thomason) is respectfully traversed and should be withdrawn.

O'Connor concerns a method of time shifting to simultaneously record and play a data stream (Title). Yonemitsu concerns methods and devices for encoding and decoding frame signals and recording medium therefore (Title). Russo concerns a video time-shifting apparatus (Title). Thomason concerns an arrangement for storing an information signal in a memory and for retrieving the information signal from said memory (Title).

Claim 1 provides (in part) steps for (i) a first buffering of an input signal having a digital video format and (ii) compressing the input signal in parallel with the first buffering. In contrast, the combined teachings of O'Connor and Yonemitsu, as suggested in the Office Action, appear to perform a compression sequentially after a first buffering. Therefore, O'Connor and Yonemitsu, alone or in combination, do not teach or suggest steps for (i) a first buffering of an input signal having a digital video

format and (ii) compressing the input signal in parallel with the first buffering as presently claimed.

Claim 1 further provides a step for delivering a plurality of real-time video frames along a first processing path to an output for display in response to the input signal as first buffered. In contrast, the proposed combination of O'Connor and Yonemitsu appears to be silent regarding a video in block 102 of O'Connor providing video frames **as buffered** along a bypass 142. Therefore, the Examiner is respectfully requested to either (i) clearly identify the column and line of O'Connor that discuss the bypass 142 carrying frames as buffered in the video in block 102 or (ii) withdraw the rejection.

The assertion on page 7 of the Office Action that buffering and compressing inherently occur substantially simultaneously is respectfully traversed and should be withdrawn. Inherency requires certainty of results, not mere possibility. See, e.g., *Ethyl Molded Products Co. v. Betts Package, Inc.*, 9 U.S.P.Q. 2d 1001 (E.D.Ky 1988). See also, *In re Oelrich*, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981). Any amount of delay may be provided between a buffer operation and a compression operation. Therefore, no certainty of results exists that the two operations must be performed substantially simultaneously. The Examiner is respectfully requested to either (i) provide evidence of the alleged inherency or (ii) withdraw the inherency assertion.

Claim 20 provides a real-time decoder configured to (i) generate a first output signal by decompressing a compressed

digital video input signal and (ii) pause a frame of the first output signal during a transition from a first mode to a second mode. In contrast, the video in block 102 of O'Connor (asserted similar to the claimed real-time decoder) does not appear to have (i) a decompression capability or (ii) a frame pause capability. Therefore, O'Connor does not teach or suggest a real-time decoder configured to (i) generate a first output signal by decompressing a compressed digital video input signal and (ii) pause a frame of the first output signal during a transition from a first mode to a second mode as presently claimed.

Furthermore, page 12 of the Office Action alleges that the bypass 142 of O'Connor is available when the input signal is a compressed video signal. In contrast, column 4, lines 54-57 of O'Connor states:

> **In one embodiment**, a bypass 142, as shown in FIG. **1**, allows the incoming video stream to be provided to the VIDEO OUT port 120 directly. (Emphasis added)

Nothing in O'Connor indicates that the bypass 142 is available for all configurations, including the compressed video input/uncompressed video output configuration asserted in the Office Action. Therefore, the Examiner is respectfully requested to either (i) provide a clear and concise explanation why one of ordinary skill in the art would consider the bypass 142 of O'Connor to apply to a compressed video input situation or (ii) withdraw the rejection.

Furthermore, the Office Action provides no evidence of motivation to modify O'Connor as required by MPEP §2142. First, no

evidence is provided why one of ordinary skill in the art would be motivated to add a decompression capability to the video in block 102 of O'Connor. Second, no evidence is provided why one of ordinary skill in the art would be motivated to combine the video in block 102 of O'Connor (asserted decompression) with the video out block 120 of O'Connor (asserted frame pause). The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness (MPEP §2143.01). Therefore, *prima facie* obviousness has not been established. The Examiner is respectfully requested to either (i) clearly identify the source of motivation, and if knowledge generally available to one of ordinary skill in the art, provide evidence of such knowledge or (ii) withdraw the rejection.

Claim 21 provides a frame buffer directly connected to an input (for receiving a video signal in an uncompressed format) and configured to (i) generate a first output signal by buffering the video signal and (ii) pause the first output signal at a frame during a transition from a first mode to a second mode. In contrast, the Office Action admits that Thomason does not disclose a frame buffer as presently claimed.

Furthermore, no evidence of motivation is provided in the Office Action to add a frame buffer to Thomason. The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness (MPEP §2143.01). Therefore, the Examiner is respectfully requested to either (i) provide evidence of motivation or (ii) withdraw the rejection.

Assuming, *arguendo*, that a frame buffer were added to Thomason after the channel selector block 1 (for which Applicants' representative does not necessarily agree), the resulting structure does not match the claim. In particular, claim 21 provides an encoder configured to generate a first intermediate signal by compressing the video signal (received at an input). However, the resulting structure teaches a data compression block 3 of Thomason (asserted similar to the claimed encoder) receiving a signal from the newly added frame buffer instead of the channel selector 1 (asserted similar to the claimed input). Therefore, the proposed modification of Thomason does not appear to teach or suggest an encoder configured to generate a first intermediate signal by compressing the video signal as presently claimed.

Claim 21 further provides a controller configured to (i) receive a first intermediate signal, (ii) present a second intermediate signal and (iii) generate a command. In contrast, page 16 of the Office Action asserts that one of ordinary skill in the art would consider a buffer 4 of Thomason to be similar to the claimed controller. EEdesign (www.eedesign.com) defines "controller" and "buffer" very differently:

> Controller - An electronic system that directs the operation of some larger system.
>
> Buffer - An isolation circuit used to insulate sensitive analog or digital circuits from higher-power or higher-current levels in other portions of an electronic design. Often seen, for example as an I/O buffer which separates the sensitive circuits inside of an IC from the signals on the circuit board to which the IC is attached.

Therefore, one of ordinary skill in the art would not appear to consider the buffer 4 of Thomason similar to the claimed controller. As such, the Examiner is respectfully requested to either (i) provide evidence that one of ordinary skill in the art would consider the buffer 4 of Thomason to be similar to a controller or (ii) withdraw the rejection.

Claim 21 further provides a frame storage system directly connected to the controller and configured to (i) store a first intermediate signal and (ii) generate a second intermediate signal. In contrast, FIG. 1 of Thomason shows that a buffer memory 35 (asserted similar to the claimed frame storage system) is **indirectly** connected to a buffer 4 (asserted similar to the claimed controller) through a DMA controller 31. Therefore, Thomason does not appear to teach or suggest a frame storage system **directly** connected to the controller and configured to (i) store a first intermediate signal and (ii) generate a second intermediate signal as presently claimed.

Claim 21 further provides the controller is configured to generate a command configured to control presenting (i) a first output signal (generated by a frame buffer) when in a first mode and (ii) a second output signal (generated by a time-shifted decoder) when in a second mode. Assuming, *arguendo*, that a frame buffer was added to the design of Thomason (for which Applicants' representative does not necessarily agree), nothing in the proposed modified design appears to teach or suggest a first output signal from the frame buffer being presented while in a first mode.

Therefore, the Examiner is respectfully requested to either (i) clearly and precisely identify where Thomason discusses (a) the claimed first mode, (b) the claimed second mode, (c) the claimed command and (d) presentation of the claimed first output signal when in the first mode or (ii) withdraw the rejection.

Claim 22 provides a real-time decoder configured to (i) generate a first output signal in response to decompressing a video input signal (in a compressed format) and (ii) pause a frame of the first output signal during a transition from a first mode to a second mode. In contrast, the video in block 102 of O'Connor (asserted similar to the claimed real-time decoder) does not appear to have (i) a decompression capability or (ii) a frame pause capability. Therefore, O'Connor does not teach or suggest a real-time decoder configured to (i) generate a first output signal in response to decompressing a video input signal (in a compressed format) and (ii) pause a frame of the first output signal during a transition from a first mode to a second mode as presently claimed.

Furthermore, page 13 of the Office Action alleges that the bypass 142 of O'Connor is available when the input signal is a compressed video signal. In contrast, column 4, lines 54-57 of O'Connor states:

> **In one embodiment**, a bypass 142, as shown in FIG. 1, allows the incoming video stream to be provided to the VIDEO OUT port 120 directly. (Emphasis added)

Nothing in O'Connor indicates that the bypass 142 is available for all configurations, including the compressed video input/uncompressed video output configuration asserted in the

Office Action. Therefore, the Examiner is respectfully requested to either (i) provide a clear and concise explanation why one of ordinary skill in the art would consider the bypass 142 of O'Connor to apply to a compressed video input situation or (ii) withdraw the rejection.

Furthermore, the Office Action provides no evidence of motivation to modify O'Connor as required by MPEP §2142. First, no evidence is provided why one of ordinary skill in the art would be motivated to add a decompression capability to the video in block 102 of O'Connor. Second, no evidence is provided why one of ordinary skill in the art would be motivated to combine the video in block 102 of O'Connor (asserted decompression) with the video out block 120 of O'Connor (asserted frame pause). The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness (MPEP §2143.01). Therefore, *prima facie* obviousness has not been established. The Examiner is respectfully requested to either (i) clearly identify the source of motivation, and if knowledge generally available to one of ordinary skill in the art, provide evidence of such knowledge or (ii) withdraw the rejection.

Claim 22 further provides a controller and a frame storage system coupled to the controller to exchange a video input signal. Assuming, *arguendo*, that a compression block 104 and a decompression block 110 of O'Connor could be combined to form a frame storage system (for which Applicants' representative does not necessarily agree), the resulting combination does not appear to

exchange a video input signal (in a compressed format) with a processor 130 of O'Connor (asserted similar to the claimed controller). In particular, FIG. 1 of O'Connor shows **no exchange** of video between the compression block 104 and/or decompression block 110 of O'Connor with the processor 130. Furthermore, the video signal presented by the decompression block 110 of O'Connor is not in a compressed format. Therefore, the Examiner is respectfully requested to either (i) provide a clear and concise explanation (a) how the compression block 104 and the decompression block 110 of O'Connor exchange a compressed video input signal with the processor 130 and (b) how the compression block 104 compresses an already compressed video signal (necessitating the addition of a decompression capability to the video in block 102 for the bypass 142) or (ii) withdraw the rejection.

Claim 23 provides a first frame buffer configured to (i) generate a first signal and a second signal by buffering an input signal, (ii) pause the first signal at a frame during a transition from a real-time mode to a time-shifted mode and (iii) buffer a third signal. In contrast, Thomason appears to be silent regarding a frame buffer configured to buffer both an input signal and a third signal as presently claimed. Therefore, the Examiner is respectfully requested to either (i) identify (a) a frame buffer of Thomason allegedly similar to the claimed first frame buffer and (b) signals of Thomason allegedly similar to the claimed first signal, the claimed second signal and the claimed third signal or (ii) withdraw the rejection.

Claim 23 further provides (i) an encoder connected to the first frame buffer and configured to generate the third signal by compressing the second signal. In contrast, Thomason appears to be silent regarding an encoder connected to a first frame buffer and configured to generate a third signal (buffered by the first frame buffer) by decompressing a second signal (received from the first frame buffer) as presently claimed. Therefore, the Examiner is respectfully requested to either (i) identify where Thomason allegedly discusses a frame buffer, an encoder, a second signal and a third signal as claimed or (ii) withdraw the rejection.

Claim 23 further provides a controller connected to the first frame buffer to receive the third signal. In contrast, Thomason appears to be silent regarding a controller receiving a signal buffered in the first frame buffer. Therefore, the Examiner is respectfully requested to either (i) identify where Thomason allegedly discloses a controller receiving a third signal from a frame buffer or (ii) withdraw the rejection.

Claim 23 further provides a buffer connected to the controller to store the third signal. In contrast, Thomason appears to be silent regarding a buffer storing a signal received from a frame buffer through a controller. Therefore, the Examiner is respectfully requested to either (i) clearly identify a circuit in Thomason allegedly similar to the claimed buffer or (ii) withdraw the rejection.

Claims 23 further provides a switch connected to the first frame buffer and configured to present an output signal comprising (i) the first signal when in a real-time mode and (ii)

a fourth signal when in a time-shifted mode. In contrast, Thomason appears to be silent regarding a switch as presently claimed. Therefore, the Examiner is respectfully requested to either (i) identify a circuit in Thomason allegedly similar to the claimed switch or (ii) withdraw the rejection.

Claim 4 provides a transition from a real-time mode to a time-shifted mode is triggered by a single command of a viewer. Despite the assertion on page 4 of the Office Action, O'Connor appears to contemplate two user commands to transition between modes. For example, FIG. 7 of O'Connor illustrates a first user input 702 to transition from a real-time to a paused condition and a second user input 706 to transition from the paused to a time-delayed condition. Therefore, O'Connor and Yonemitsu, alone or in combination, do not teach or suggest a transition from a real-time mode to a time-shifted mode is triggered by a single command of a viewer as presently claimed. As such, the Examiner is respectfully requested to either (i) provide a clear and concise explanation how a transition from a read-time mode to a paused-mode triggers a transition from the real-time mode to a time-shifted mode or (ii) withdraw the rejection.

Claim 8 provides that real-time video frames are provided from a decoder that decompresses an input signal. Page 10 of the Office Action alleges that the bypass 142 of O'Connor is available when the input signal is a compressed video signal and therefore a decoder is implied in the video in block 102. In contrast, column 4, lines 54-57 of O'Connor states:

> **In one embodiment**, a bypass 142, as shown in FIG. 1, allows the incoming video stream to be provided to the VIDEO OUT port 120 directly. (Emphasis added)

Nothing in O'Connor indicates that the bypass 142 is available for all configurations, including the compressed video input/uncompressed video output configuration asserted in the Office Action. Therefore, the Examiner is respectfully requested to either (i) provide a clear and concise explanation why one of ordinary skill in the art would consider the bypass 142 of O'Connor to apply to a compressed video input situation or (ii) withdraw the rejection.

Claim 11 provides that the transition is from a particular real-time video frame to a next frame (in display sequence after the particular real-time video frame) of time-shifted video frames. Despite the assertion on page 5 of the Office Action, each of O'Connor, Yonemitsu and Russo appear to be silent regarding a transition from one frame from the real-time frames to a subsequent frame from the time-shifted frames. Therefore, O'Connor, Yonemitsu and Russo, alone or in combination, do not teach or suggest a transition from a particular real-time video frame to a next frame of time-shifted video frames as presently claimed. As such, the Examiner is respectfully requested to either (i) quote the language of Russo allegedly stating that a RESUME command begins with "a next frame" or (ii) withdraw the rejection.

Furthermore, no evidence of motivation to combine the references is provided in the Office Action. In particular, the

alleged motivation on page 12 of the Office Action is not credited to any reference or knowledge generally available to one of ordinary skill in the art. Therefore, *prima facie* obviousness has not been established. The Examiner is respectfully requested to either (i) identify the source of the alleged motivation, and if knowledge generally available, provide evidence of such knowledge or (ii) withdraw the rejection.

Claim 29 provides a second frame buffer disposed between a controller, a time-shifted decoder and a switch. In contrast, Thomason appears to be silent regarding a second frame buffer as presently claimed. Therefore, the Examiner is respectfully requested to either (i) identify a frame buffer in Thomason allegedly similar to the claimed second frame buffer or (ii) withdraw the rejection.

COMPLETENESS OF THE OFFICE ACTION

Aside from a notice of allowance, Applicants' representative respectfully requests any further action on the merits be presented as a non-final action. 37 CFR §1.104(b) states:

> (b) *Completeness of examiner's action.* The examiner's **action will be complete as to all matters**, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

No arguments were developed for independent claim 23 and dependent claim 29. Despite the assertion on page 18 of the Office

Action, claims 23 and 29 include structures and signals not found in claims 21 and 28. Therefore, the Action mailed August 12, 2004 was not complete. If the differences between claims 21 and 23 are "merely minor variations in schematics" as asserted by the Examiner, then the Examiner is respectfully requested to cut-and-paste the arguments for claim 21 into the rejection of claim 23 with the appropriate changes so that Applicants' representative has a clear understanding of the rejection for claim 23.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana
Registration No. 42,829

Dated: November 9, 2004

c/o Henry Groth
LSI Logic Corporation
1621 Barber Lane, M/S D-106 Legal
Milpitas, CA 95035

Docket No.: CC-084/CPA / 1496.00251